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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	-	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/118,359	07/17/1998	J. DENNIS KELLER		MI22-587	8927
21567	7590	07/26/2005		EXAMINER	
WELLS ST. JOHN P.S. 601 W. FIRST AVENUE, SUITE 1300 SPOKANE, WA 99201				ESTRADA, MICHELLE	
				ART UNIT	PAPER NUMBER
				2823	

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/118,359

Applicant(s)

KELLER ET AL.

Examiner

Michelle Estrada

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 April 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 91-103 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 91-103 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 91-103 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Araki et al. (5,882,994) and Koido (2001/0014530).

Araki et al. disclose forming an oxide-comprising layer (103) against and physically contacting a semiconductive substrate (101); forming a first layer (104 doped) over the oxide-comprising layer, wherein the first layer comprises a semiconductive material and a dopant; after forming the first layer, forming a second layer (104) against and physically contacting the first layer, wherein the second layer comprises semiconductive material, the semiconductive material of the second layer having less dopant than the semiconductive material of the first layer; forming a third layer (106) over the second layer, the third layer comprising dielectric material; forming a fourth layer (107) over the third layer, the fourth layer comprising conductive material; etching the oxide-comprising layer and the first through fourth layers to form a plurality of floating gates (Col. 4, line 58-62); and forming an oxide layer over the floating gates (Col. 5, lines 3-5).

Araki et al. do not disclose that the first layer comprising semiconductive material and a dopant physically contacts the oxide-comprising layer.

Araki et al. disclose that when the memory cell is formed using phosphorus within the floating gate is diffused into the cell gate oxide film, which results in structural damage within the cell gate oxide film. It invokes, a problem concerning reliability due to an increase on the leak current (Col. 1, lines 57-64). Phosphorus in polysilicon is diffused into the bottom oxide film during oxidation of polysilicon, which results in the degradation of the bottom oxide film quality (Col. 1, line 66-Col. 2, line 2). The structure of this invention can effectively decrease the damage caused by the impurity, especially in the case of the cell gate oxide film (Col. 4, lines 33-35). It is easy to avoid damage to the cell gate oxide film in the oxidation process (Col. 4, lines 49-50). It is possible not only to prevent damage to the cell gate oxide film due to the impurity in polysilicon, but it is also possible to control the bottom oxide film and minimize the natural oxide film formation (Col. 5, lines 36-39). These teachings indicate that the disclosed formation of an undoped layer contacting the gate dielectric is merely desirable as opposed to necessary to produce a working device.

Furthermore, there is no indication that the device would be inoperable using a doped polysilicon layer contacting the gate dielectric. Araki et al. statements are a preferable embodiment. It would have been obvious to employ a doped semiconductive material in contact with the oxide-comprising layer with the expectation that Araki's disclosed advantages would not be obtained. One of ordinary skill in the art would have had a reasonable expectation of success when employing a doped semiconductive material in contact with the oxide-comprising layer.

The disclosed examples and preferred embodiments do not constitute a teaching away from a broader disclosure or nonpreferred embodiments. In *re Susi*, 169 USPQ 423 (CCPA 1971). "A known or obvious composition does not become patentable simply because it has been described as somewhat inferior to some other product for the same use." In *re Gurley*, 31 USPQ2d 1130, 1132 (Fed. Cir. 1994). A reference may be relied upon for all that it would have reasonably suggested to one having ordinary skill in the art, including nonpreferred embodiments. *Merck & Co. v. Biocraft Laboratories*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989). Even a teaching away from a claimed invention does not render the invention patentable. See *Celeritas Technologies Ltd. v. Rockwell International Corp.*, 150 F.3d 1354, 1361, 47 USPQ2d 1516, 1522-23 (Fed. Cir. 1998), where the court held that the prior art anticipated the claims even though it taught away from the claimed invention. "The fact that a modem with a single carrier data signal is shown to be less than optimal does not vitiate the fact that it is disclosed." To further clarify, a prior art opinion that a claimed invention is not preferred for a particular limited purpose, does not preclude utility of the invention for that or another purpose, or even preferability of the invention for another purpose.

Araki et al. do not disclose disposing a plug of conductive contact film operatively adjacent at least one of the drain regions, the plug of conductive material being electrically connected to the at least one of the drain regions.

Koido discloses forming floating gates; forming an oxide layer (7) over the source and drain regions and the floating gates; and disposing a plug of conductive contact

Art Unit: 2823

(17a) film operatively adjacent at least one of the drain regions, the plug of conductive material being electrically connected to the at least one of the drain regions (Page 5, Paragraph [0063]).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Araki et al. and Koido to enable the plug formation step of Koido to be performed in the process of Araki et al. to provide electrical connection between the drain and any subsequent layer formed, e.g. wiring layer or interconnection layer.

With respect to claims 93 and 94, Araki discloses a thickness of the first layer (inner portion) of silicon to be 70 nm and a thickness of 70 nm for the second layer (outer portion) of silicon (Col. 3, lines 30-32). Araki does not disclose the specifically recited thickness ranges of the instant application, however, the disclosed range overlaps with the claimed range in the instant application of a thickness for the inner portion to comprise at least 25%, between 25% and 75%, and less than 75% of the material thickness. (See MPEP 2144.05).

With respect to claims 95 and 96, Araki discloses a dopant concentration of $1 \times 10^{20} \text{cm}^{-3}$ in the first layer and a dopant concentration of none in the second layer (Col. 5, lines 14-17). Araki does not disclose the specifically recited dopant concentration of the instant application, however, the range disclosed by Araki overlaps with the claimed range in the instant application of a concentration equal to or greater than $1 \times 10^{18} \text{cm}^{-3}$ in the first portion and less than $1 \times 10^{18} \text{cm}^{-3}$ in the second portion. (See MPEP 2144.05).

With respect to claim 97, the method of claim 97 merely describes the effect of doping the first layer with a higher concentration of impurity than the second layer. Araki discloses forming a second layer of polysilicon to have a lower dopant concentration than the first layer. Araki does not explicitly disclose that this process of doping results in a greater sheet resistance in the second layer than in the first layer. Wolf teaches that undoped polysilicon exhibit high sheet-resistivity values while doped polysilicon exhibits a lower the resistivity (Silicon Processing Vol. 2 pages 581). It would have been within the scope of one of ordinary skill in the art at the time of the invention that doping the second layer of polysilicon with a lower concentration of impurity than the first would result in a the second layer possessing a higher sheet resistance and would achieve the results of Araki.

With respect to claims 98, Araki discloses a dopant concentration of $1 \times 10^{20} \text{ cm}^{-3}$ in the first layer of polysilicon (Col. 5, lines 14-17). This range overlaps with the claimed range in the instant application of greater than or equal to $1 \times 10^{18} \text{ cm}^{-3}$ for the first layer. Araki also discloses a thickness of the first layer (inner portion) of silicon to be 70 nm and a thickness of 70 nm for the second layer (outer portion) of silicon (Col. 3, lines 30-32). This range overlaps with the claimed range in the instant application of a thickness for the inner portion to occupy less than 75% of the floating gate thickness. (See MPEP 2144.05).

With respect to claim 99, Araki discloses wherein the third layer (106) comprises nitride (Col. 4, line 53).

With respect to claim 100, Araki discloses first and second thicknesses of the first and second polysilicon layers to be 70 nm and 70 nm respectively. Araki does not disclose the specifically recited thicknesses of the instant application, however, the range disclosed by Araki overlaps with the claimed range in the instant application of a being substantially the same (Col. 3, lines 30-32). (See MPEP 2144.05).

With respect to claim 101, Araki discloses first and second thicknesses of the polysilicon layers (Col. 3, lines 30-32). Araki fails to teach the first and second thicknesses being different. However, given the substantial teaching of Araki, it would have been obvious to one with ordinary skill in the art at the time of the invention to determine the optimal thicknesses for the first and second layers through routine experimentation and optimization to achieve optimum benefits including transistor performance (See MPEP 2144.05).

With respect to claims 102 and 103, Araki discloses a first polysilicon layer 70 nm thick and a second layer of polysilicon 70 nm thick. Araki does not disclose the specifically recited thicknesses of between 450 Angstroms and 550 Angstroms. However, given the substantial teaching of Araki, it would have been obvious to one with ordinary skill in the art at the time of the invention to determine the optimal thicknesses for the first and second layers through routine experimentation and optimization to achieve optimum benefits including transistor performance (See MPEP 2144.05).

Response to Arguments

Applicant's arguments filed 4/25/05 have been fully considered but they are not persuasive. Applicant request the Examiner to direct him to the teaching of the element of the first layer including semiconductive material and a dopant, and at least some of the dopant contacting the oxide-comprising layer. As explained before, Araki discloses that the function of the bottom layer of the semiconductive material is to make easier to avoid damage to the cell gate oxide film. The damage decreases reliability due to increase leak current (Col. 1, lines 60+). Therefore this disclosure is merely preferable. One of ordinary skill in the art would have had a reasonable expectation of success forming an undoped layer and then a doped layer because Araki discloses separate advantages associated with use of the undoped layers and also because the bottom portion of the electrode would then be as in the prior art method described in claim 1 wherein the floating gate is uniformly doped. Furthermore, one of ordinary skill in the art would have had a reasonable expectation of success forming an undoped layer and then a doped layer with the expectation that the advantages of Araki would not be obtained.

Applicant argues that the middle layer 104 cannot be confused with the first layer as recited in claim 91 for at least the reason that it does not physically contact the oxide-comprising layer. However, the rejection is based omitting the first layer and using the middle layer physically contacting the oxide-comprising layer with the expectation that you would not obtain the advantages of Araki's first layer.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michelle Estrada whose telephone number is 571-272-1858. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2800.

Art Unit: 2823

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Michelle Estrada
Patent Examiner
Art Unit 2823

ME
July 23, 2005